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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,361	PARK, WON-KI	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-14 and 16-22* is/are rejected.

7)☒ Claim(s) *8 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a reply to Applicant's restriction election filed 08/22/2005. The Applicant elected claims 8-22 and accordingly withdrew claims 1-7 from consideration.

Claim Objections/Minor Informalities

1. Claim 8 is objected to because of the following informalities:

Claim 8, lines 1 and 4, it is suggested to change "adapted" to --configured-- to reflect positive limitations.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (U.S. Patent No. 6,552,587).

With respect to claim 8, Kim et al. discloses, in Figs. 4 and 6, a replica delay circuit configured for use in an internal clock generator, the replica delay circuit receiving an external clock signal [Fig. 4, ext_clk] and outputting an internal clock *(Fig. 4, output from item 700)*, and comprising a circuit configured to synchronize a phase difference between the external clock signal and a reference clock signal, wherein the internal clock signal is derived in relation to the phases difference *(Fig. 4, output from item 400)*; a first replica delay unit *(Fig. 6, item 101)* , delaying the internal clock signal for a predetermined period of time and generating first delay clock signals; and a second replica delay unit *(Fig. 6, items 102, 111, 112, 121, 122)*, generating the reference clock signal *(Fig. 4, output from item 100)* in response to the first delay clock signals and changing a duty cycle of the reference clock signal in response to selected control signals *(Fig. 6, items fd1, fd2, bd1, bd2)*.

4. Claim 15 is rejected under 35 U.S.C. 102(e) as being anticipated by Yang (U.S. Patent No. 6,754,841).

With respect to claim 15, Yang discloses, in Fig. 1, an internal clock generator receiving an external clock signal [Ckref] and generating an internal clock signal *(output of item 2)* in relation to a phase difference determined in relation to a phase/delay lock comparison between the external clock signal and an internally generated reference clock signal, the internal clock generator comprising a variable delay circuit [top VCDL] delaying the external clock signal for a first predetermined period of time and generating a delayed external clock signal, a buffer circuit [2] amplifying the delayed external clock signal and generating the internal clock signal, a replica delay circuit [bottom VCDL] delaying the internal clock signal for a second

predetermined period of time, generating the reference clock signal *(output of bottom VCDL)*, and changing a duty cycle of the reference clock signal in response to control signals *(output of item CP)*, a control signal generator [CP] generating the control signals in accordance with a phase offset between the internal clock signal and the external clock signal, and a phase detector [PD] detecting a phase difference between the external clock signal and the reference clock signal and controlling the first predetermined amount of time of the variable delay circuit in accordance with a detection result.

Allowable Subject Matter

5. Claims 9-14 and 16-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A replica delay circuit, in which the second replica delay unit further comprises a first amplifier generating second delay clock signals in response to the first delay clock signals and changing a common mode voltage level for the second delay clock signals in response to the selected control signals; and a second amplifier, comparing voltage levels for the second delay clock signals, outputting the reference clock signal in accordance with a comparison result, and changing the duty cycle of the reference clock signal in accordance with changes in the common mode voltage level of the second delay clock signals, as called for in claim 9; and

b) An internal clock generator, in which the second replica delay unit further comprises

a first replica delay unit delaying the internal clock signal for a third predetermined period of time and generating first delay clock signals, and a second replica delay unit generating the reference clock signal in response to the first delay clock signals and changing a duty cycle of the reference clock signal in response to control signals, as called for in claim 16.

Citation of Relevant Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Cho (U.S. Patent No. 6,518,807) discloses a mixed delay locked loop circuit.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LINH MY NGUYEN
PRIMARY EXAMINER